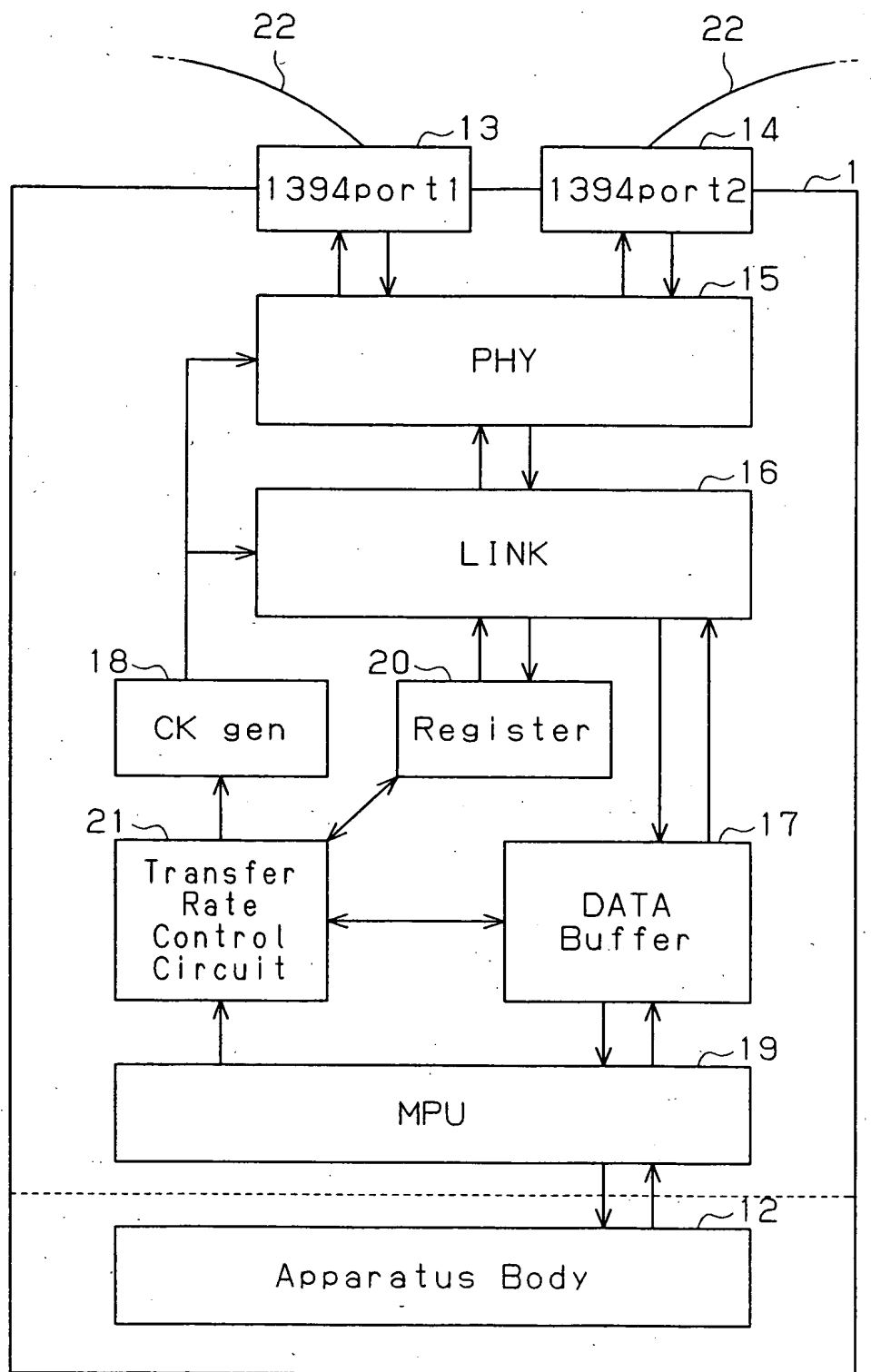


Fig.1



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Fig. 2

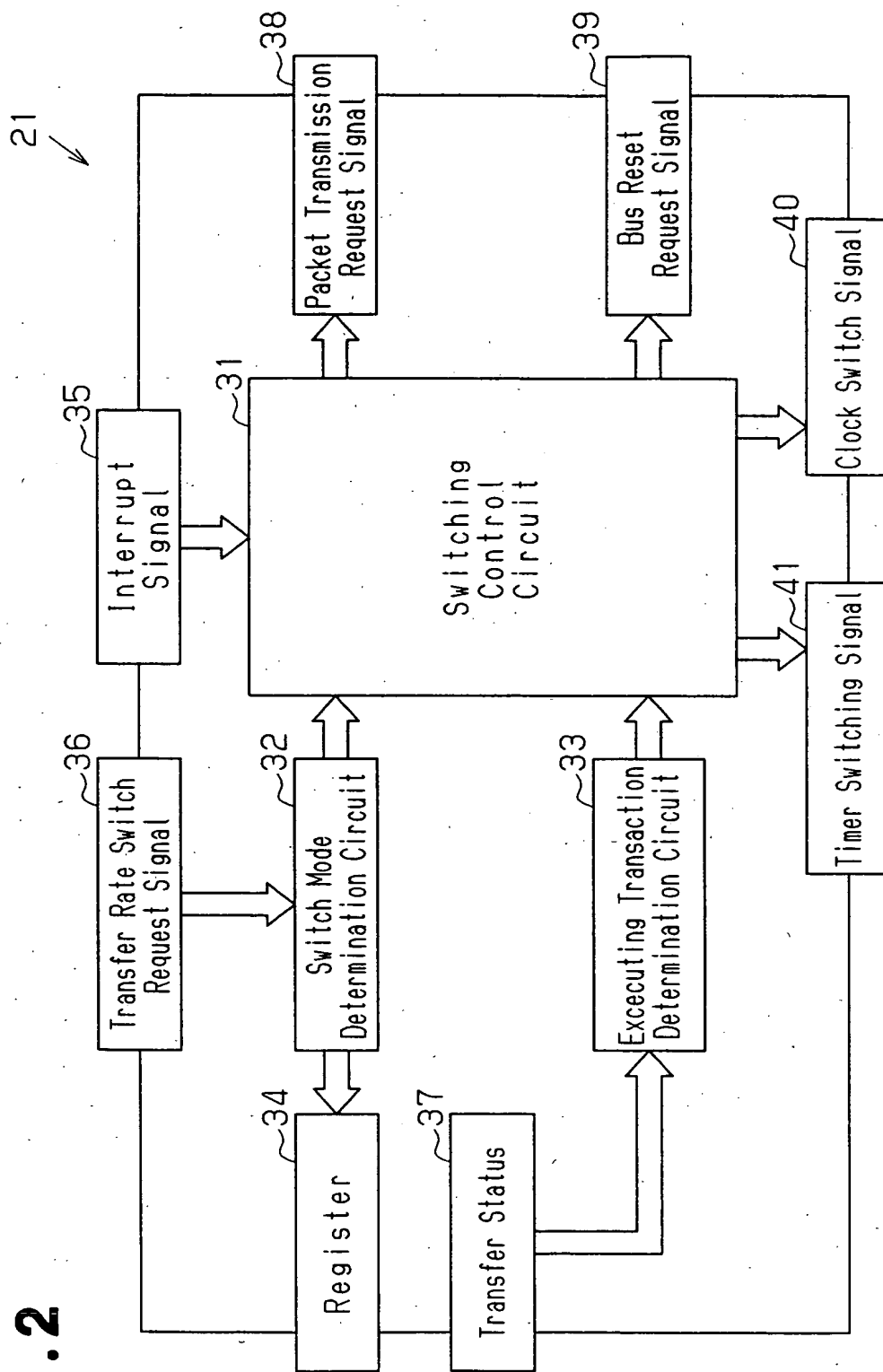


Fig. 3

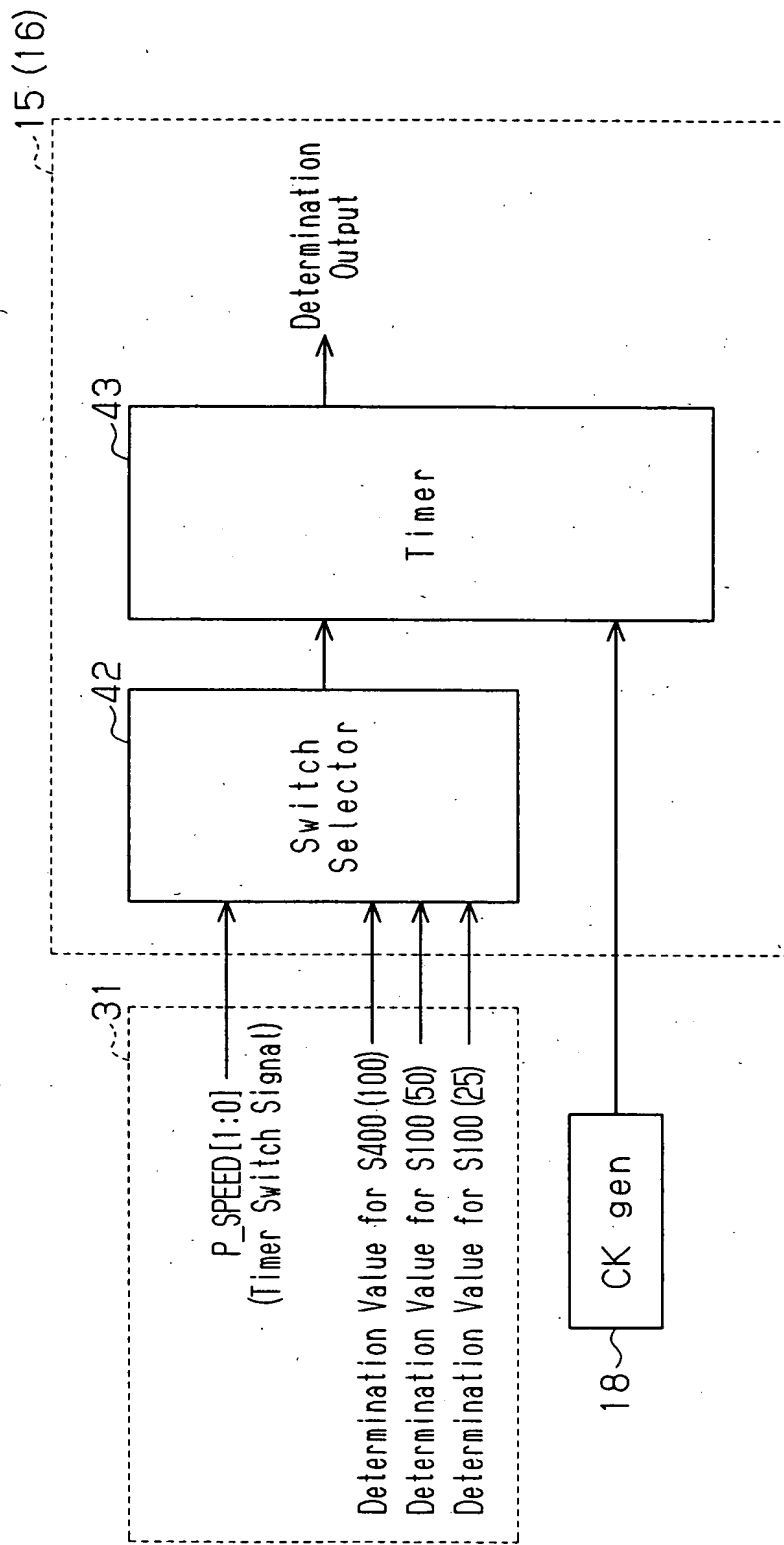


Fig.4

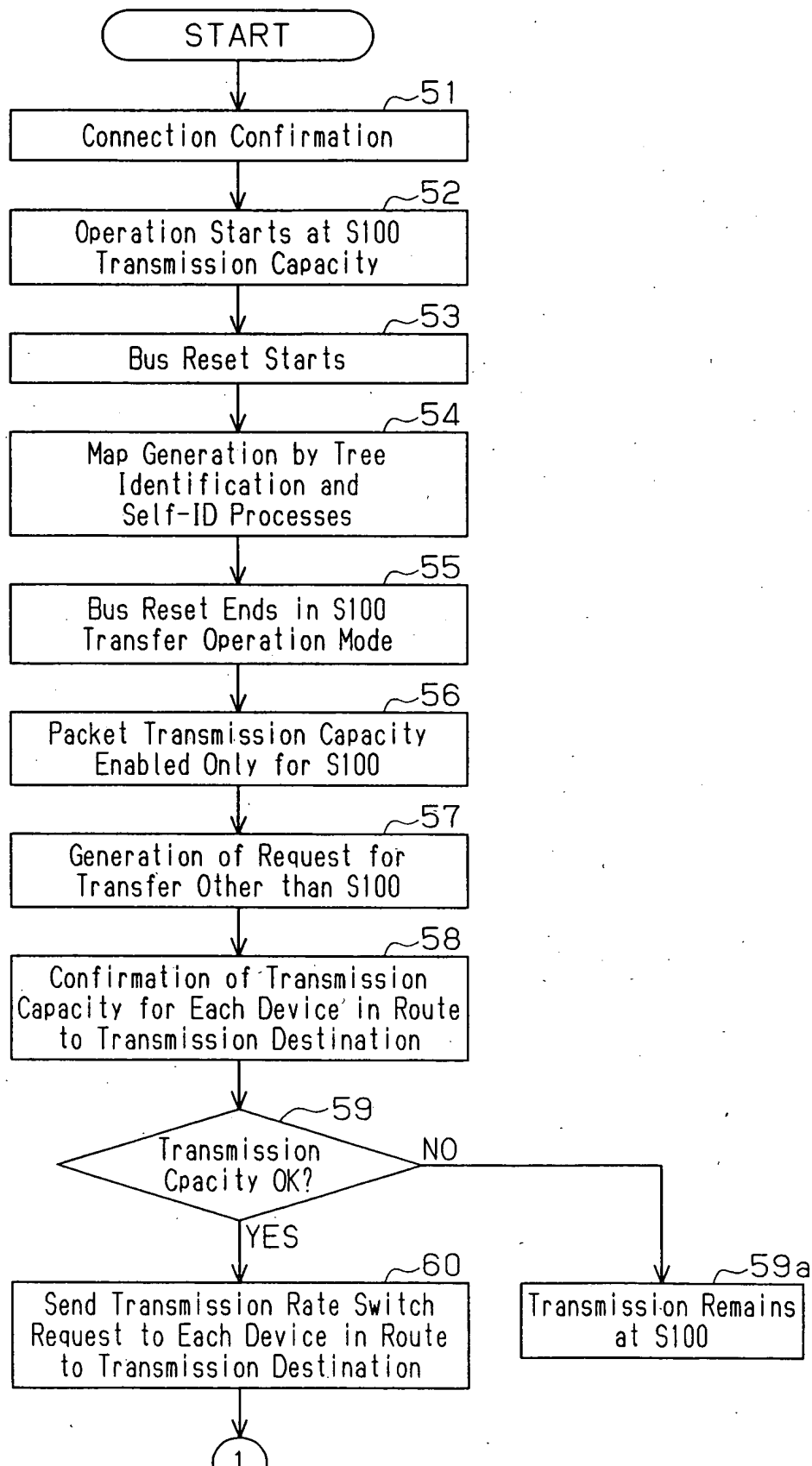


Fig.5

Transmission Rate Switch
Request Sending Side

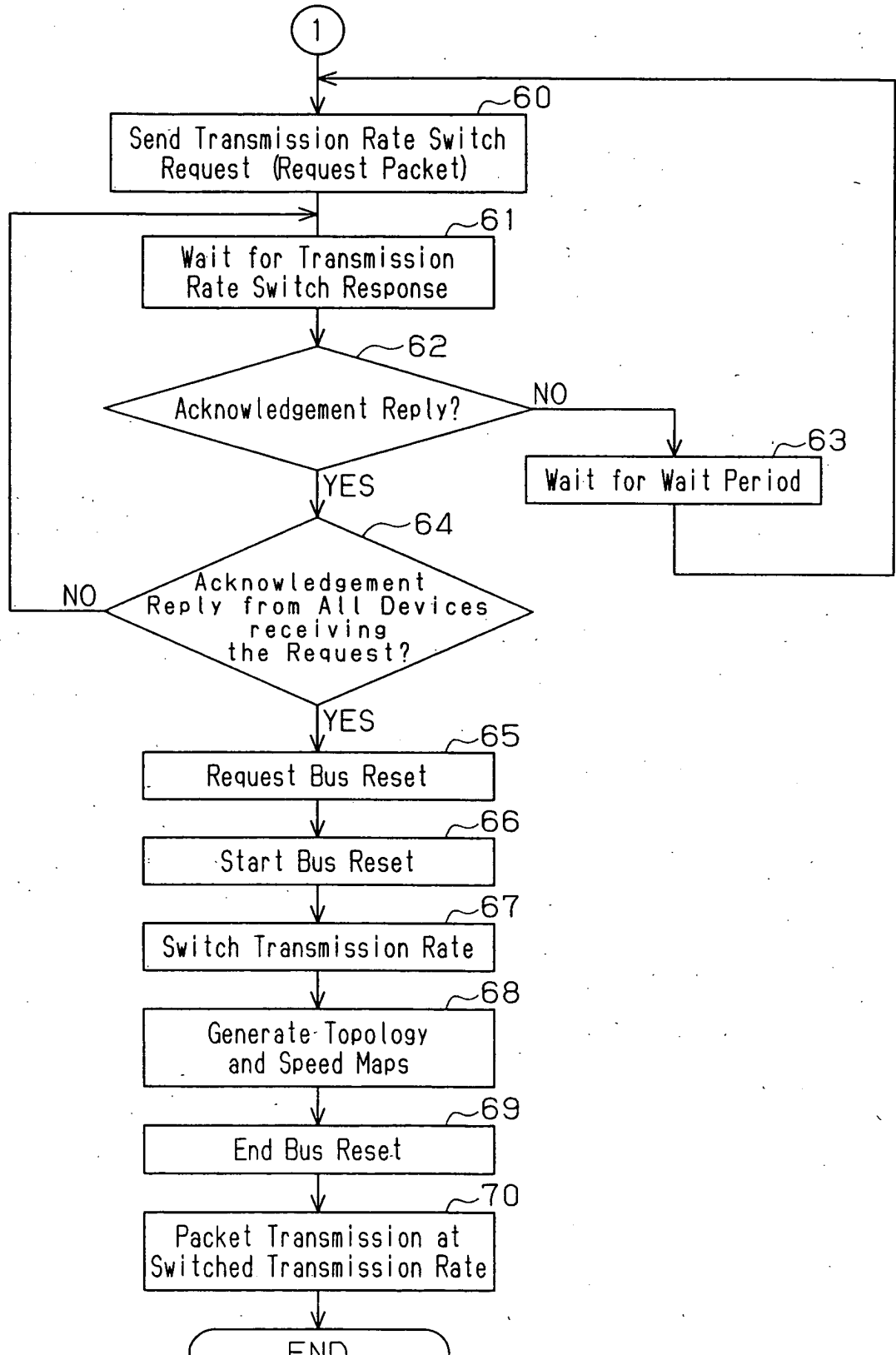


Fig.6

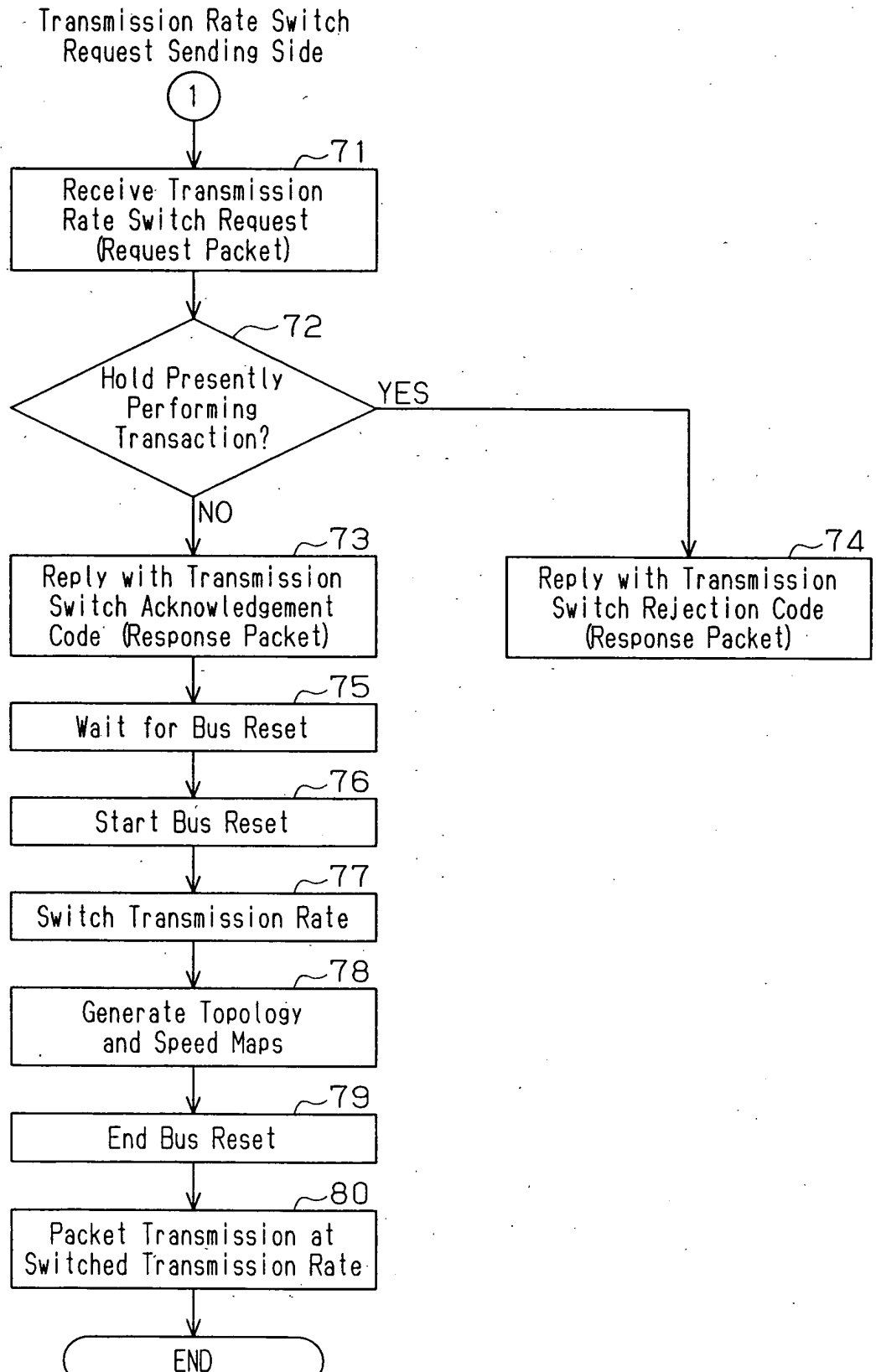


Fig.720

Register Abbreviation	Description
20a C_SPEED	Display Device Transmission Capacity
	00:S100
	01:S200
	1x:S400
20b P_SPEED	Current Operating State
	00:S100
	01:S200
	1x:S400
20c N_SPEED	Operating State after Next Bus Reset
	00:S100
	01:S200
	1x:S400
20d CHG_MODE	0:Clear for Each Bus Reset
	1:Do Not Clear for Each Bus Reset

Fig.8

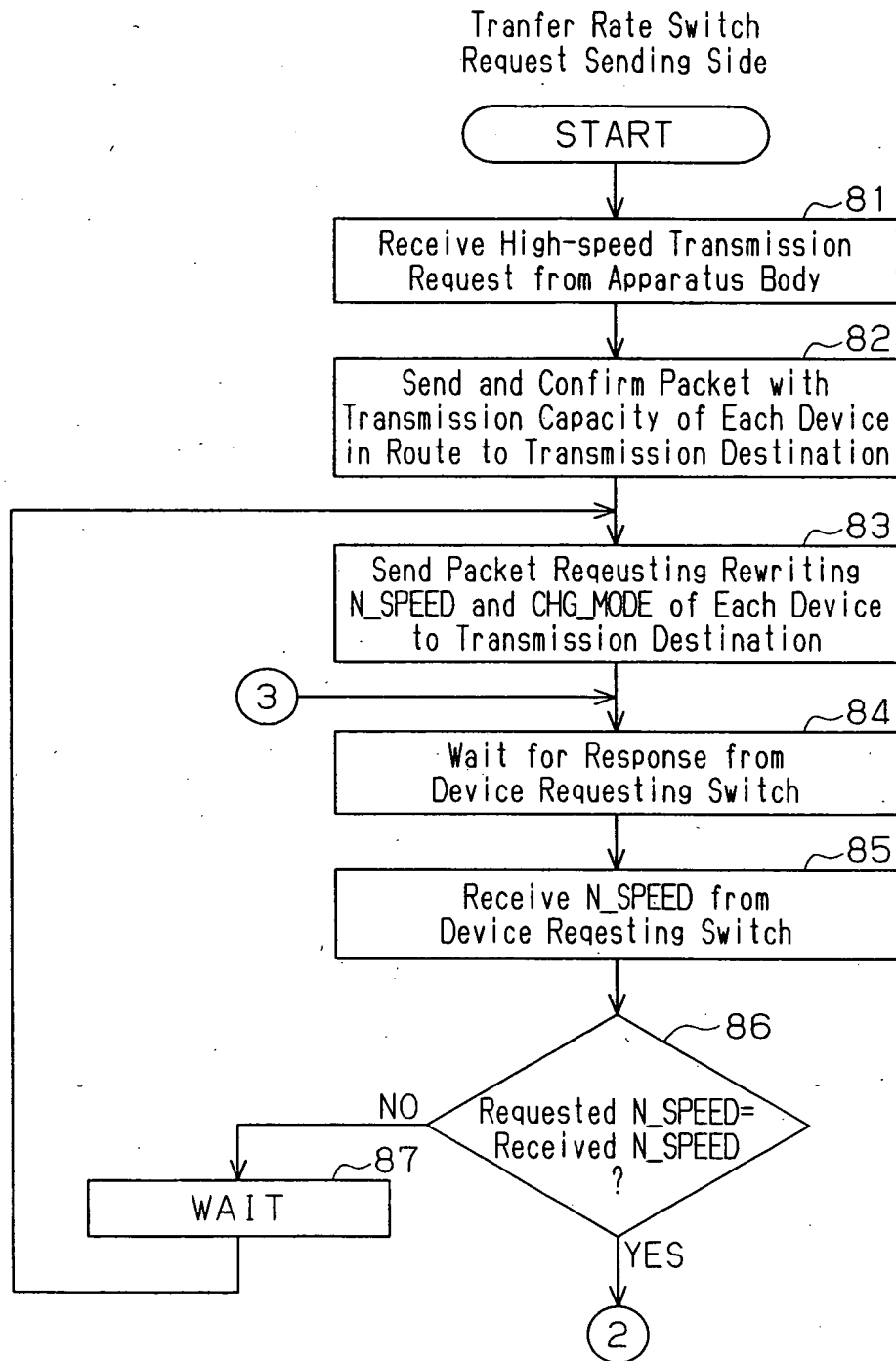


Fig. 9

Transmission Rate Switch
Request Sending Side

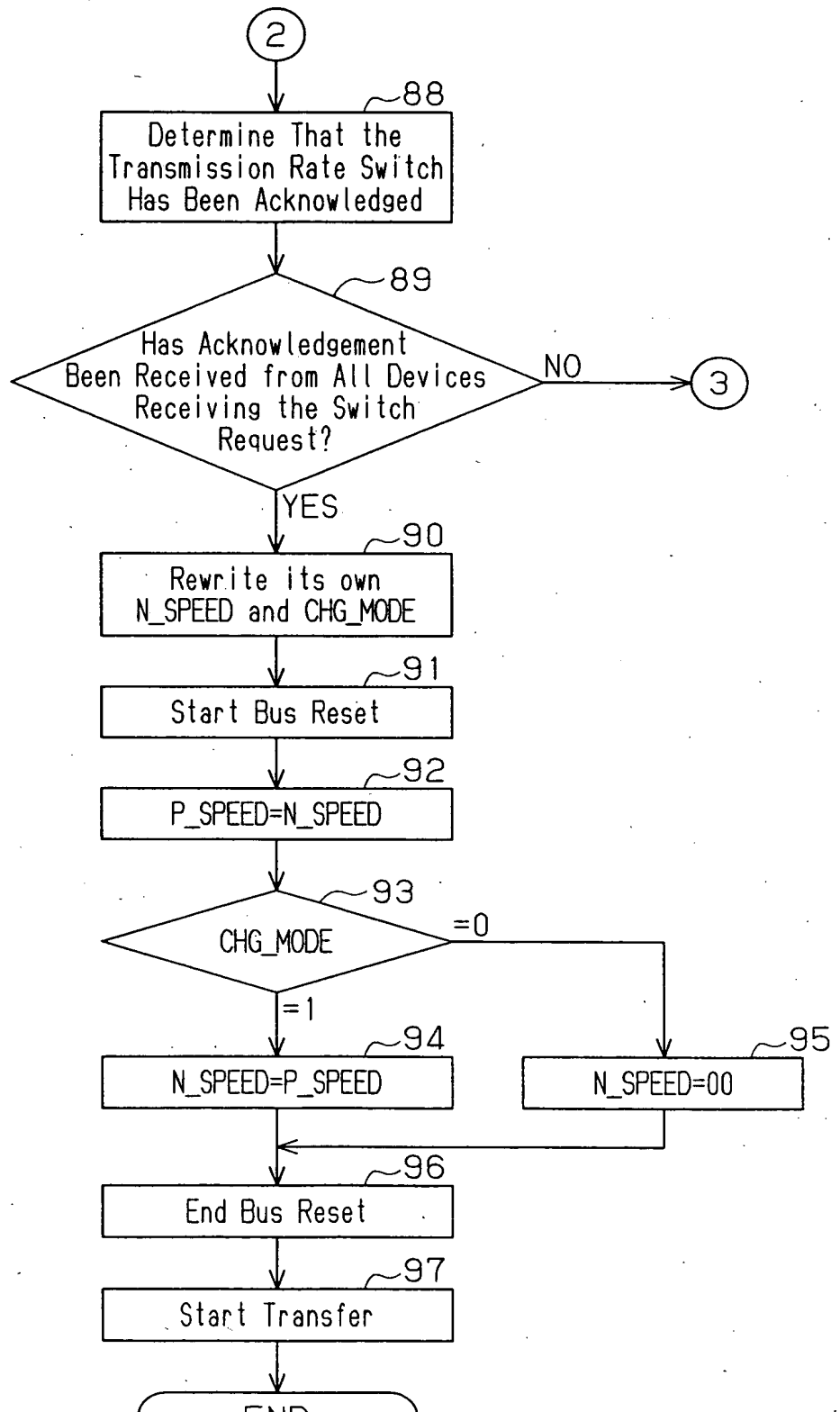


Fig.10

Transfer Rate Switch
Request Receiving Side

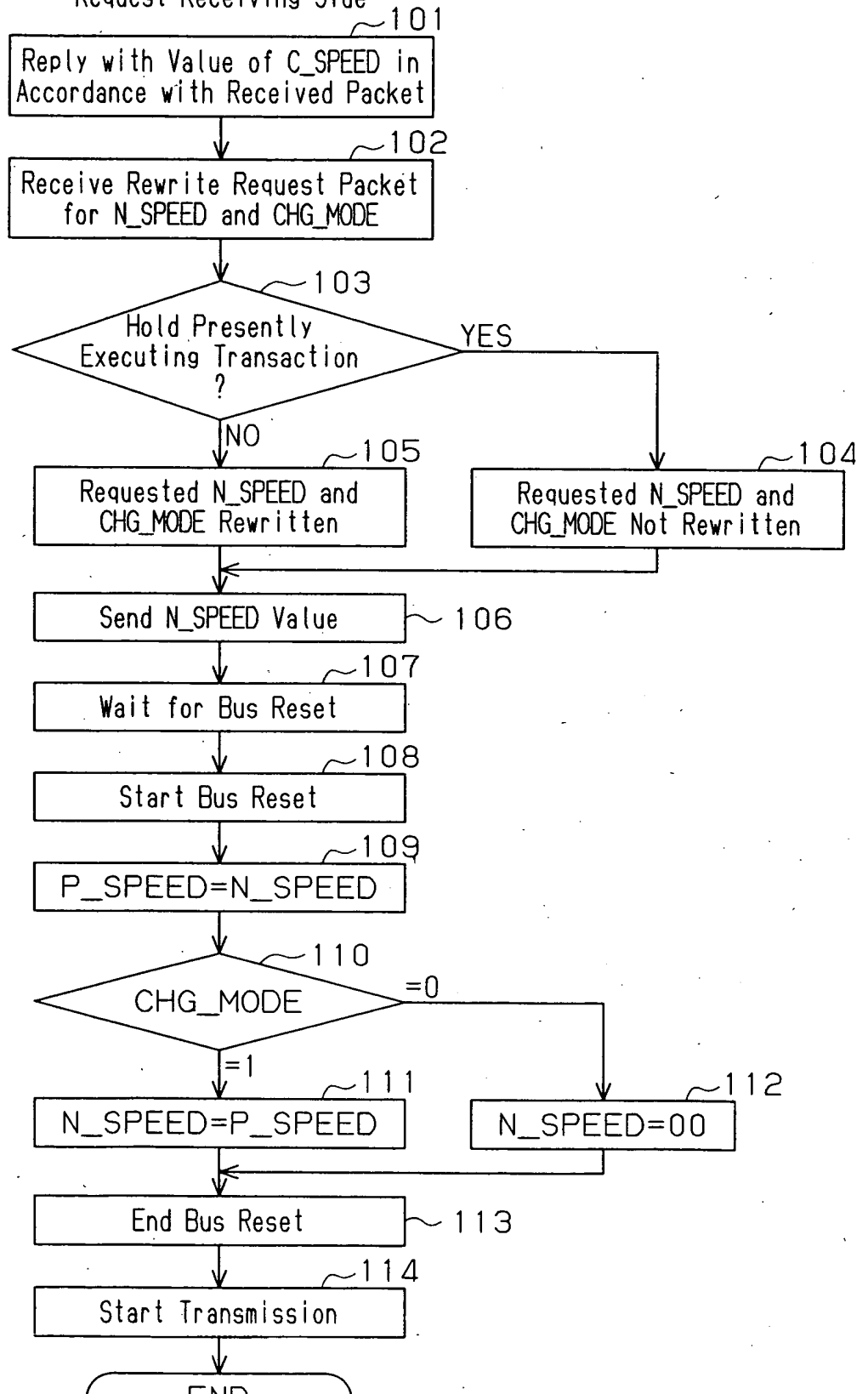


Fig.11

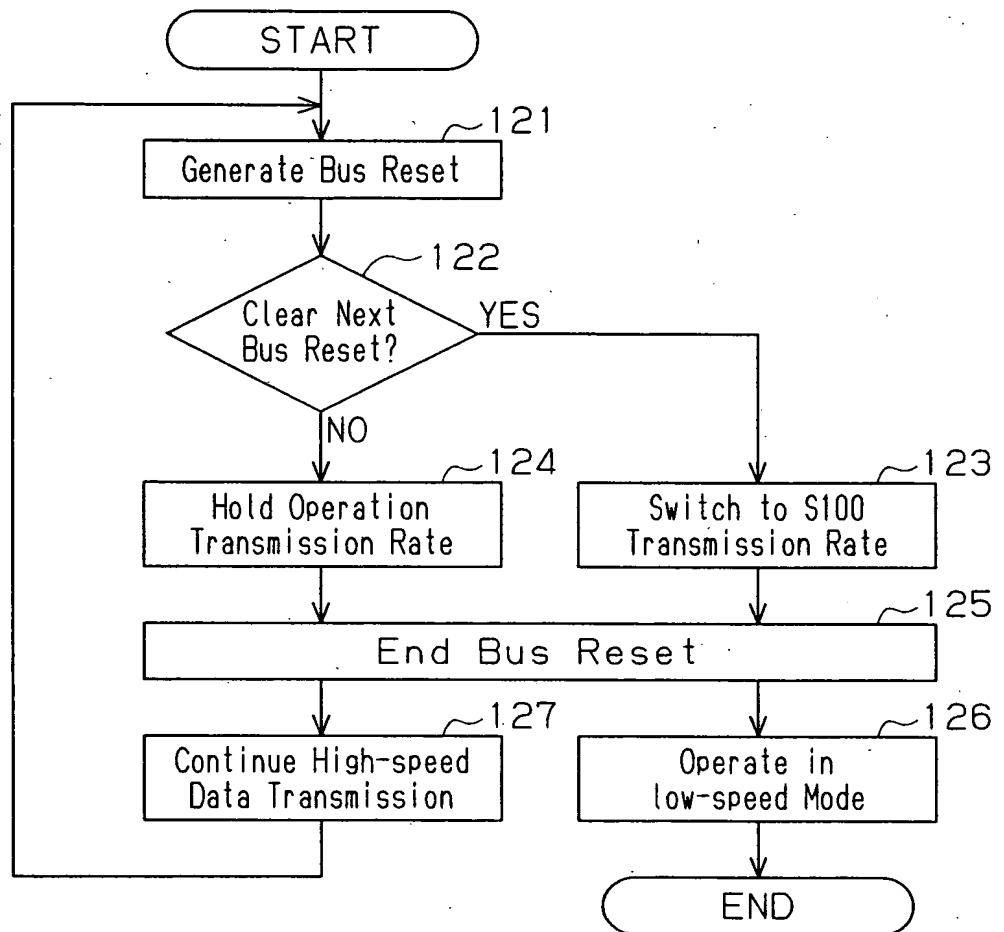


Fig.12 (Prior Art)

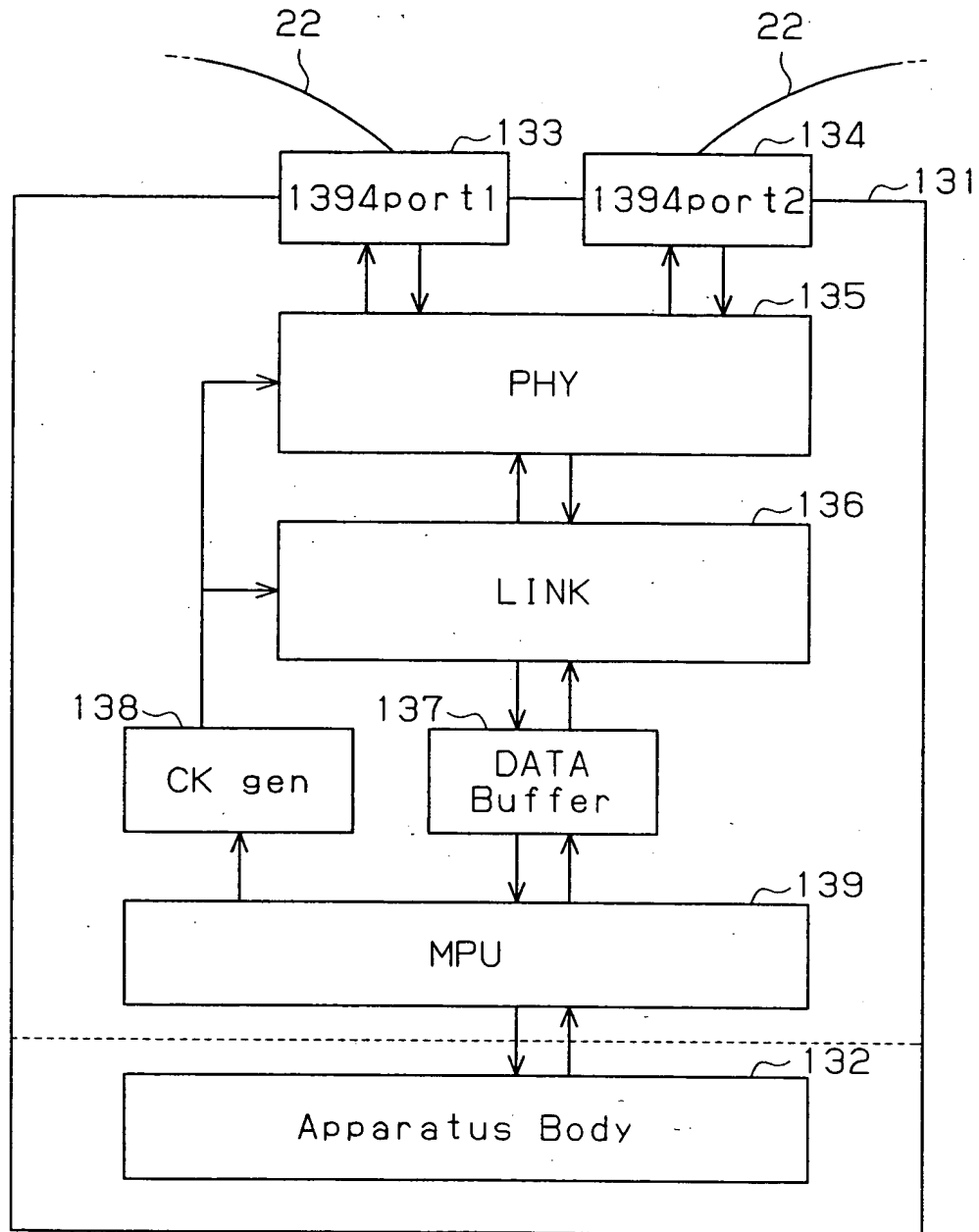
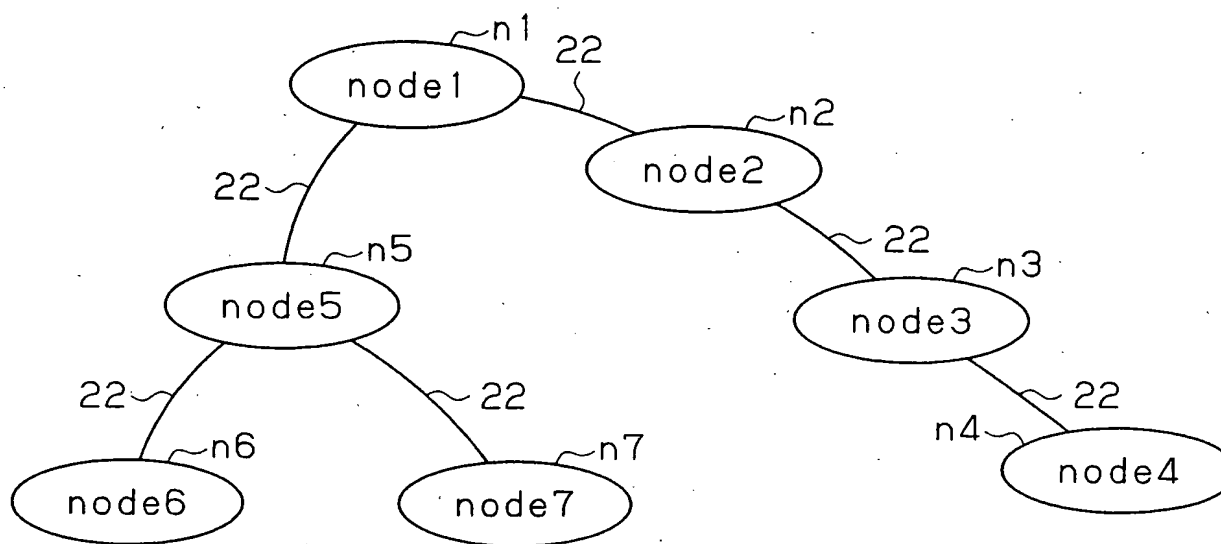


Fig.13 (Prior Art)



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